REMARKS

Reconsideration and allowance of this application are respectfully requested. Claims 1, 4, 9, 10 and 12-15 have been amended. Support for the claim amendments is found in the specification in at least paragraphs [0035] and [0036] and FIGS. 4-9. Claims 1-15 are pending in the application. The rejections are respectfully submitted to be obviated in view of the amendments and remarks presented herein.

As a preliminary matter, Applicants traverse the finality of the Office Action dated June 23, 2008. The Examiner indicates that, although the claims are now subject to new grounds of rejection (paragraph 12 on page 12 of the Office Action), the new grounds of rejection are allegedly necessitated by the Applicants' amendment (paragraph 13 on page 13 of the Office Action).

However, a second or any subsequent action on the merits in any application should not be made final if it includes a rejection, on prior art not of record, of any claim amended to include limitations which should reasonably have been expected to be claimed (see MPEP §§ 706.07(a) and 904 *et seq*). The Amendments to the claims (Amendment filed on April 2, 2008) were all made according to the Examiner's suggestions or of an editorial nature to correct minor informalities. Such amendments editorial in nature and according to the Examiner's suggestions to correct minor claim informalities would not necessitate the new grounds of rejection presented in the present Office Action. Accordingly, Applicants respectfully request that the finality of the Office Action dated June 23, 2008 be withdrawn.

Rejection Under 35 U.S.C. § 112, Second Paragraph

Claims 9, 10 and 12-15 have been rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicants have editorially amended claims 9, 10 and 12-15 to improve clarity. In particular, as described in the specification as exemplary embodiments of the present invention, and taken in conjunction with that which is shown in at least FIGS. 4-9, "the length of said field plate portion does not exceed 70% of an interval between said gate electrode and said drain electrode," and also, "the length of said field plate portion that extends to said drain electrode is 0.5 μm or more and preferably 0.7 μm or more."

Reconsideration and withdrawal of the rejection under 35 U.S.C. § 112, second paragraph, are respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Claims 1, 2, 4, 6-10 and 12-15, as best understood, have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over newly cited Toshimoto (JP 56088364) in view of Shur et al. (U.S. Patent No. US 2005/0087752; hereinafter "Shur"). The rejection is respectfully traversed.

Regarding claim 1, claim 1, as amended, recites a field effect transistor comprising:

a III group nitride semiconductor layer structure including hetero junction;

a source electrode and a drain electrode that are so formed on said semiconductor layer structure as to be separated from each other;

a gate electrode formed on said semiconductor layer and between said source electrode and said drain electrode; and

an insulating film formed on said semiconductor layer structure,

wherein said gate electrode has a field plate portion that projects towards said drain electrode in the form of an eave and that is formed on said insulating film; and

wherein a thickness of a portion of said insulating film lying between said field plate portion and said semiconductor layer structure gradually increases from said gate electrode toward said drain electrode.

Although Toshimoto discloses an insulated gate field effect transistor (IGFET) semiconductor device as shown in FIG. 1 and described in the abstract, Toshimoto's IGFET fails to teach or suggest "a gate electrode **formed on said semiconductor layer** and between said source electrode and said drain electrode," as recited by amended claim 1 (emphasis added). As shown in Toshimoto's FIG. 1, a gate electrode (12) is formed on a gate insulating film (c), the gate insulating film (c), a drain electrode (13) and a source electrode (14) being formed on a substrate (8). As such, because Toshimoto's gate electrode (12) is formed on the gate insulating film (c) and not on the substrate (8), Toshimoto thus fails to teach or suggest "a gate electrode formed on said semiconductor layer," as recited by amended claim 1.

Furthermore, as conceded by the Examiner in paragraph 7 on page 4 of the Office Action, "Toshimoto does not state the semiconductor structure is a III group nitride semiconductor layer structure including hetero junction."

Shur does not remedy the deficiencies of Toshimoto. As shown in FIG. 5 of Shur, a gate (222) is formed on a dielectric second layer (218). As such, Shur also fails to teach or suggest "a gate electrode formed on said semiconductor layer," as recited by amended claim 1.

Furthermore, both Toshimoto and Shur are directed towards a completely different structure than the claimed invention. Exemplary embodiments of the present invention refer to a gate electrode which is arranged in Schottky contact and which has a field plate portion that projects to a drain electrode in the form of an eave and is formed on an insulating film. Contrarily, Toshimoto and Shur refer to a metal-insulator-semiconductor (MIS) type gate structure.

Exemplary embodiments of the present invention aim to enhance the gate breakdown voltage and to suppress collapse by reducing concentration of the electric field to the gate edge between the gate and the drain. On the other hand, Toshimoto and Shur are both directed towards very different devices . As such, the claimed invention is very different from both Toshimoto and Shur in purpose and structure. Therefore, due at least to this deficiency in both Toshimoto and Shur, the claimed invention is distinguished over Toshimoto in view of Shur.

For at least the aforementioned reasons, claim 1, as amended, is distinguished over Toshimoto in view of Shur. Claim 4 is a related apparatus claim which is also distinguished over Toshimoto in view of Shur for analogous reasons. Claims 2, 6-10 and 12-15 are dependent claims which are also distinguished over Toshimoto in view of Shur at least in view of their dependencies as well as for their additionally recited elements.

With further regard to claim 8, "a drain field plate electrode connected to said drain electrode is arranged on said insulating film between said gate electrode and said drain electrode." The Examiner alleges in paragraph 7 on page 4 of the Office Action that "the prior art combined device shows a drain field plate electrode 13 (left portion) connected to said drain electrode 13 (right portion) is arranged on said insulating film 11 between said gate electrode 12 and said drain electrode 13 (right portion) (Toshimoto: Fig. 2)." However, Toshimoto's drain

electrode (13) is one element having a uniform consistency, and Toshimoto is silent on the drain electrode (13) having a right portion and a left portion, the left portion being arranged on the insulating film (11). Although a part of Toshimoto's drain electrode (13) covers the insulating film (11), such part of the drain electrode (13) is not taught or suggested to be a drain field plate electrode, but instead, is only disclosed by Toshimoto to be one element mounted in the drain region (9). For at least the aforementioned reasons as well as for these additional differences, claim 8 is distinguished over Toshimoto in view of Shur.

With further regard to claims 9 and 10, the Examiner alleges that it would have been obvious to have the size of the field plate portion not exceed 70% of an interval between the gate electrode and the drain electrode, "in order to optimize the performance of the device." However, the Examiner has relied upon improper hindsight in citing this conclusion. Also, as Toshimoto's gate electrode (12) is provided as shown in FIG. 2, it is unclear as to what the Examiner interprets as a field plate portion, because Toshimoto's gate electrode (12) is a uniform element, and therefore there lacks any teaching or suggestion that a portion of such gate electrode (12) does not exceed 70% of the interval between the remaining portion of the gate electrode (12) and the drain electrode (13). Furthermore, it is disclosed in a non-limiting exemplary embodiment of the present invention in paragraph [0036] of the specification, that "when the end portion of field plate portion 5 at the side of drain electrode 3 exceeds 70% of the interval between gate electrode 2 and drain electrode 3, the gate breakdown voltage is adversely apt to be lowered." For at least the aforementioned reasons as well as for these additional differences, claims 9 and 10 are distinguished over Toshimoto in view of Shur.

With further regard to claims 12-15, the Examiner also alleges that it would have been obvious to have the entire size of the field plate portion that extends to the drain electrode to be

0.5 μm or more and preferably 0.7 μm or more, "in order to optimize the performance of the device." However, the Examiner has again relied upon improper hindsight in citing this conclusion. For at least the aforementioned reasons as well as for these additional differences, claims 12-15 are distinguished over Toshimoto in view of Shur.

Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

Claim 11 has been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Toshimoto and Shur in view of newly cited Riccobene (U.S. Patent No. 6,229,184). The rejection is respectfully traversed.

As discussed above, claim 1 is distinguished over Toshimoto in view of Shur. Riccobene does not remedy the deficiencies of Toshimoto in view of Shur. Riccobene shows in FIG. 1 a gate electrode (13) formed on a gate dielectric layer (11), and therefore Riccobene's gate electrode (13) is not formed on a semiconductor layer. Furthermore, the Examiner concedes that Toshimoto and Shur do not disclose "a thickness of said field plate portion gradually decreases from said gate electrode toward said drain electrode."

The Examiner alleges in paragraph 8 on page 7 of the Office Action that "Riccobene teaches a thickness of said field plate portion gradually decreases from said gate electrode towards said drain electrode (Fig. 1)." However, as shown in FIG. 1 of Riccobene, it is clearly shown that the thickness of the gate electrode (13) ***increases*** towards the drain region (15 and 16). Therefore, Riccobene fails to teach or suggest "wherein a thickness of said field plate portion gradually decreases from said gate electrode towards said drain electrode," as recited by claim 11.

As such, claim 1 is distinguished over Toshimoto and Shur in view of Riccobene. Claim 11 is a dependent claim, and is also distinguished over Toshimoto and Shur in view of Riccobene at least in view of its dependency as well as for its additionally recited elements.

Claims 1-3, 6-9, 12 and 14, as best understood, have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shirai (U.S. Patent No. 5,422,505) in view of Shur. The rejection is respectfully traversed.

Neither Shirai nor Shur, either alone or in combination, teach or suggest the claimed invention as recited by amended claim 1.

Shirai fails to teach or suggest, *inter alia*, "a gate electrode formed on said semiconductor layer and between said source electrode and said drain electrode," as recited by amended claim 1. As shown in Shirai's FIG. 1, Shirai's gate electrode (G) is formed on a gate insulating film (14), and not on the semiconductor substrate (10). As is also conceded by the Examiner in paragraph 9 on page 8 of the Office Action, "Shirai does not state that semiconductor structure is a III group nitride semiconductor layer structure including hetero junction."

Shur does not remedy the deficiencies of Shirai. As discussed above, Shur also fails to teach or suggest "a gate electrode formed on said semiconductor layer and between said source electrode and said drain electrode," as recited by amended claim 1.

Furthermore, both Shirai and Shur are directed towards a completely different structure than the claimed invention. Exemplary embodiments of the present invention refer to a gate electrode which is arranged in Schottky contact and which has a field plate portion that projects to a drain electrode in the form of an eave and is formed on an insulating film. Contrarily, Shirai and Shur refer to a metal-insulator-semiconductor (MIS) type gate structure.

Exemplary embodiments of the present invention aim to enhance the gate breakdown voltage and to suppress collapse by reducing concentration of the electric field to the gate edge between the gate and the drain. On the other hand, Shirai aims to realize a uniform distribution of an electric field in MOSFET by varying the thickness of the gate insulating film of the MIS type gate structure. As such, the claimed invention is very different from both Shirai and Shur in purpose and structure. Therefore, due at least to this deficiency in both Shirai and Shur, the claimed invention is distinguished over Shirai in view of Shur.

For at least the aforementioned reasons, claim 1, as amended, is distinguished over Shirai in view of Shur. Claims 2, 3 and 6-9, 12 and 14 are dependent claims which are also distinguished over Shirai in view of Shur for at least their dependencies as well as for their additionally recited elements.

With further regard to claim 8, "a drain field plate electrode connected to said drain electrode is arranged on said insulating film between said gate electrode and said drain electrode." The Examiner alleges in paragraph 9 on page 9 of the Office Action that "the prior art combined device shows a drain field plate electrode D2 connected to said drain electrode D is arranged on said insulating film 14 between said gate electrode G and said drain electrode D (Shirai: Fig. 1)." However, Shirai's drain electrode (13) is one element having a uniform consistency, and although the drain electrode (13) is formed partly on the interlayer insulating film (15), Shirai is silent on also including a drain field plate electrode, but instead, Shirai's drain electrode (D) is only disclosed to be formed on both the interlayer insulating film (15) and the drain region (12) of the semiconductor substrate (10). For at least the aforementioned reasons as well as for these additional differences, claim 8 is distinguished over Shirai in view of Shur.

With further regard to claim 9, the Examiner alleges that it would have been obvious to have the size of the field plate portion not exceed 70% of an interval between the gate electrode and the drain electrode, "in order to optimize the performance of the device." However, the Examiner has relied upon improper hindsight in citing this conclusion. As discussed above, it is disclosed in a non-limiting exemplary embodiment of the present invention in paragraph [0036] of the specification, that "when the end portion of field plate portion 5 at the side of drain electrode 3 exceeds 70% of the interval between gate electrode 2 and drain electrode 3, the gate breakdown voltage is adversely apt to be lowered." For at least the aforementioned reasons as well as for these additional differences, claim 9 is distinguished over Shirai in view of Shur.

With further regard to claims 12 and 14, the Examiner also alleges that it would have been obvious to have the entire size of the field plate portion that extends to the drain electrode to be 0.5 μm or more and preferably 0.7 μm or more, "in order to optimize the performance of the device." However, the Examiner has again relied upon improper hindsight in citing this conclusion. For at least the aforementioned reasons as well as for these additional differences, claims 12 and 14 are distinguished over Shirai in view of Shur.

Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

Claim 5 has been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shirai and Shur in view of Martinez et al. (U.S. Patent No. US 2003/0235974). The rejection is respectfully traversed.

As discussed above, neither Shirai nor Shur, either alone or in combination, teach or suggest the claimed invention as recited by amended claim 1.

Martinez discloses an RF enhancement mode FET as shown in FIG. 3. However, Martinez also fails to teach or suggest, *inter alia*, "a gate electrode formed on said semiconductor layer and between said source electrode and said drain electrode," as recited by amended claim 1.

For at least the aforementioned reasons, claim 1, as amended, is distinguished over Shirai and Shur in view of Martinez. Claim 5 is a dependent claim which is also distinguished over Shirai and Shur in view of Martinez for at least its dependency as well as for its additionally recited elements.

Claim 11 has been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shirai and Shur in view of Riccobene. The rejection is respectfully traversed.

As discussed above, Shirai and Shur, either alone or in combination, do not teach or suggest the claimed invention as recited by amended claim 1.

Riccobene does not remedy the deficiencies of Shirai in view of Shur. Riccobene shows in FIG. 1 a gate electrode (13) formed on a gate dielectric layer (11), and therefore Riccobene's gate electrode (13) is not formed on a semiconductor layer. Furthermore, the Examiner concedes that Shirai and Shur do not disclose "a thickness of said field plate portion gradually decreases from said gate electrode toward said drain electrode."

The Examiner alleges in paragraph 11 on page 12 of the Office Action that "Riccobene teaches a thickness of said field plate portion gradually decreases from said gate electrode towards said drain electrode (Fig. 1)." However, as shown in FIG. 1 of Riccobene, it is clearly shown that the thickness of the gate electrode (13) ***increases*** towards the drain region (15 and 16). Therefore, Riccobene fails to teach or suggest "wherein a thickness of said field plate

portion gradually decreases from said gate electrode towards said drain electrode," as recited by claim 11.

As such, claim 1 is distinguished over Shirai and Shur in view of Riccobene. Claim 11 is a dependent claim, and is also distinguished over Shirai and Shur in view of Riccobene at least in view of its dependency as well as for its additionally recited elements.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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